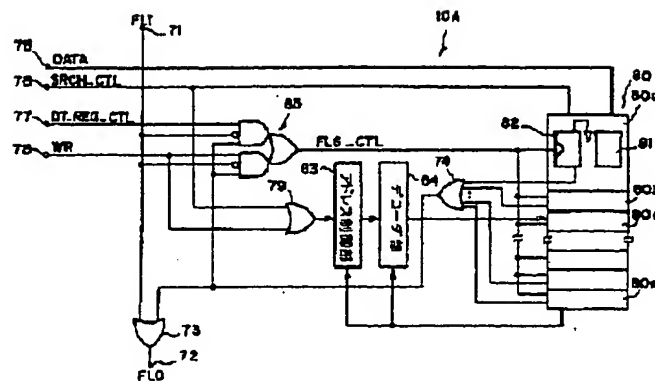


## Patent Abstracts of Japan

TITLE : ASSOCIATIVE MEMORY



**CONSTITUTION:** One 10A of plural associative memories connected in cascade retrieves using the input DATA, and stores the DATA in the memory words of memory areas 8a in a free state. Then, a gate circuit 85 inputs a data register control signal (DT-REG-CTL)A, and outputs/does not output a flag control signal (FLG-CTL)B according to the presence of priority of data register. A free flag register 82 in the area 8a having the memory word 81 storing the DATA shows storage/free state of the effective DATA according to the presence of the signal B. Thus, the retrieval and the write are performed simultaneously, and the unregistered data are registered at high speed, and memory capacity by cascade connection is increased.

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